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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,012	02/11/2004	Richard W. Foote	P05792	3404

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,012	FOOTE ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment, filed December 27, 2005, which amends claims 1 and 2 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 5-6, 11-12 and 18-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 5, 11 and 19 describe a PNP transistor and a PMOS transistor, where the base of the PNP transistor and gate of the PMOS transistor contain substantially identical dopants. As "P-N-P" defines the collector-base-emitter regions of the transistor, the base of the PNP transistor must inherently contain N-type dopants. The specification only discloses the NMOS transistor gate to have N-type dopants, while the PMOS transistor gate is masked (figs. 28A-D; ¶ 112). There is no disclosure of the PMOS transistor gate having the same dopant as the PNP transistor base.

Likewise, claims 6, 12, and 18 describe an NPN transistor and an NMOS transistor, where the base of the NPN transistor and gate of the NMOS transistor contain substantially identical dopants. As "N-P-N" defines the collector-base-emitter regions of the transistor, the base of the NPN transistor must inherently contain P-type dopants. The specification only discloses the PMOS transistor gate to have P-type dopants, while the NMOS transistor gate is masked (figs. 29A-D; ¶ 114). There is no disclosure of the NMOS transistor gate having the same dopant as the NPN transistor base.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 7-10, 13-17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachitano et al. '640 in view of Suda '441. Where product-by-process limitations are recited, the claims are limited only by the structure implied by the steps, not the manipulations of the steps. For example, anticipation of claim 7 does not require that the doping be performed by implantation (in-situ doping would result in the same structure); anticipation of claim 7, 13, or 16 does not require the doping be performed simultaneously; anticipation of claim 17 does not require etching to separate the source and drain (masked deposition would result in the same structure).

Sachitano et al. discloses a mixed bipolar-CMOS apparatus comprising a double-poly bipolar transistor and a double-poly metal oxide semiconductor (MOS) transistor on a substrate, wherein an extrinsic base of the bipolar transistor and a gate of the MOS transistor are formed of doped polysilicon (col. 8, lines 17-45). The reference discloses a device having NMOS and PMOS transistors (col. 1, lines 11-13; col. 7, lines 13-16), and describes mixed bipolar-CMOS devices that include both NPN or PNP devices (col. 1, lines 63-66). Sachitano et al. discloses an NMOS transistor with an N-type gate (col. 8, lines 17-22), and also discloses a PNP bipolar device (col. 1, lines 63-66) which would inherently have an N-type base and thus contain substantially identical dopants as the NMOS transistor gate. The reference discloses the substrate having an implanted region used as an intrinsic base of the bipolar transistor and lightly doped drain of the MOS transistor (col. 8, lines 45-49). Sachitano et al. also discloses an emitter of the bipolar transistor, a deep collector of the bipolar transistor, and separated source/drain regions of the MOS transistor that are all formed of doped polysilicon (col. 8, lines 42-45; col. 8, line 66 – col. 9, line 6.).

Sachitano et al. does not teach the base of a NPN bipolar transistor and the gate of a PMOS transistor to contain substantially identical dopants. Suda '441 teaches a BiCMOS device where the base of a NPN bipolar transistor and the gate of a PMOS transistor to contain substantially identical P-type dopants (col. 8, lines 14-17; col. 9, lines 59-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the P-type transistor gate of the PMOS device of Suda in

the BiCMOS process of Sachitano et al. One would have been motivated to do this because it was well known in the art that using a P-type dopant in the gate of a PMOS device would have created a voltage potential minimum at the surface, allowing the device to operate as a surface channel device and avoiding the short-channel degradation effects associated with buried channel PMOS devices having N-type gates.

Response to Arguments

6. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection as described above.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven J. Fulk
Patent Examiner
Art Unit 2891

February 3, 2006

BRADLEY K. SMITH
PRIMARY EXAMINER